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# Variable Length Dynamic Shifting Based Lfsr Multiple Scan Chain For Test Compression

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**Abstract:** *The project presents a test pattern compression method for circuits with a high number of parallel scan chains .It reduces test time while it keeps hardware overhead low. The decompression method is based on the continuous LFSR reseeding that is used in such a way that it enables LFSR lockout escaping within a small number of clock cycles. It requires a separate controlling of the LFSR de-compressor and the scan chain clock input. The paper discusses decompression effectiveness for different LFSR shapes ,scan chain lengths and number of parallel LFSR inputs . It is hardware saving to use an LFSR with the state skipping instead of using a LFSR accompanied with a phase shifter .It can designed in such a way that it uses a lower number of internal XOR gates, guarantees maximum separation between scan chains and does not introduce an extra delay on the LFSR outputs. Experimental result on benchmark circuits have shown that the presented test pattern decompression provides unreduced fault coverage and short test lengths while the hardware overhead is low comparing the designs designed with the help of nowadays industrial tools.*

## I. INTRODUCTION

The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing. Power dissipation is a challenging problem for today's System-on-Chips (SoCs) design and test. The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small. The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to 1. Automatic test equipment (ATE) [1] is the instrumentation used in external testing to apply test patterns to the CUT, to analyze the responses from the CUT, and to mark the CUT as good or bad according to the analyzed responses. External testing using ATE has a serious disadvantage, since the ATE (control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases. As the complexity of modern chips increases, external testing with ATE becomes extremely expensive. Instead, Built-In Self-Test (BIST) is becoming more common in the testing of digital VLSI circuits[2] since overcomes the problems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE.BIST [4] perform self-testing and reducing dependence on an external ATE. BIST is a Design-for-Testability (DFT) technique makes the electrical testing of a chip easier, faster, more efficient and less costly. The important to choose the proper LFSR architecture for achieving appropriate fault coverage and consume less power. Every architecture consumes different power for same polynomial.

Depending upon the desired fault coverage and the specific faults to be tested for, a sequence of test vectors (test vector suite) is developed for the CUT. It is the function of the TPG to generate these test vectors and apply them to the CUT in the correct sequence. A ROM[1] with stored deterministic test patterns, counters, linear feedback shift registers are some examples of the hardware implementation styles used to construct different types of TPGs[4] The BIST controller orchestrates the transactions necessary to perform self-test. In large or distributed BIST systems, it may also communicate with other test controllers to verify the integrity of the system as a whole. The external interface of the test controller consists of a single input and single output signal. The test controller's single input signal is used to initiate the self-test sequence. The test controller then places the CUT in test mode by activating input isolation circuitry that allows the test pattern generator (TPG) and controller to drive the circuit's inputs directly. Depending on the implementation, the test controller may also be responsible for supplying seed values to the TPG. During the test sequence, the controller interacts with the output response analyzer to ensure that the proper signals are being compared. To accomplish this task, the controller may need to know the number of shift commands necessary for scan-based testing. It may also need to remember the number of patterns that have been processed. The response of the system to the applied test vectors needs to be analyzed and a decision made about the system being faulty or fault-free. This function of comparing the output response of the CUT with its fault-free response is performed by the ORA. The ORA [3] compacts the output response patterns from the CUT [5] into a single pass/fail indication. Response analyzers may be implemented in hardware by making used of a comparator along with a ROM based lookup table that stores the fault-free response of the CUT. The use of multiple input signature registers (MISRs) is one of the most commonly used techniques for ORA implementations.

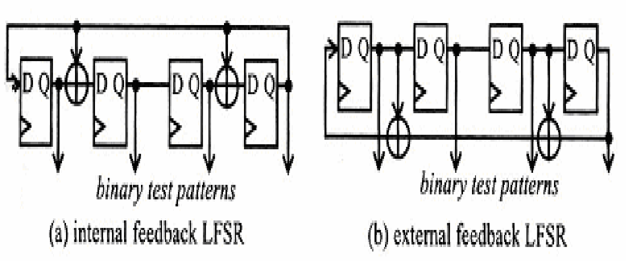
## II. RELATED WORK

The embedded deterministic test-based compression uses cube merging to reduce a pattern count, the amount of test data, and test time. It gradually expands a test pattern by incorporating compatible test cubes. In order to load scan chains with patterns that feature original test cubes, only data necessary to recreate parent patterns as well as information regarding locations and values of the corresponding conflicting bits are required. A test controller can then deliver tests by repeatedly applying the same parent pattern, every time using a different control pattern to decide whether a given scan chain receives data from the parent pattern, or another pattern is used instead to recover content of the original test cube. A novel systematic design[3] techniques for the automated register transfer level synthesis of phase shifters—circuits used to remove effects of structural dependencies featured by pseudorandom test pattern generators driving parallel scan chains. Using a concept of linear feedback shift register (LFSR) duality this paper relates the logical states of LFSRs and circuits spacing their inputs to each of the output channels. Consequently, the method generates a phase-shifter network satisfying criteria of channel separation and circuit complexity by taking advantage of simple logic simulation of the LFSRs. Many test data compression schemes are based on LFSR reseeding. A drawback of these schemes is that the unspecified bits are filled with random values resulting in a large number of transitions during scan-in thereby causing high power dissipation.

A new encoding scheme that can be used in conjunction with any LFSR reseeding scheme to significantly reduce test power and even further reduce test storage. The proposed encoding scheme acts as a second stage of compression after LFSR reseeding. It accomplishes two goals. First, it reduces the number of transitions in the scan chains (by filling the unspecified bits in a different manner), and second it reduces the number of specified bits that need to be generated via LFSR reseeding. Experimental results indicate that the proposed method significantly reduces test power and in most cases provides greater test data compression than LFSR reseeding alone A new low-power test-data-compression scheme based on linear feedback shift register (LFSR) reseeding. A drawback of compression schemes based on LFSR reseeding is that the unspecified bits are filled with random values, which results in a large number of transitions during scan-in, thereby causing high-power dissipation. A new encoding scheme that can be used in conjunction with any LFSR-reseeding scheme to significantly reduce test power and even further reduce test storage is presented. The proposed encoding scheme acts as the second stage of compression after LFSR reseeding. It accomplishes two goals. First, it reduces the number of transitions in the scan chains (by filling the unspecified bits in a different manner). Second, it reduces the number of specified bits that need to be generated via LFSR reseeding. Experimental results indicate that the proposed method significantly reduces test power and in most cases provides greater test-data compression than LFSR reseeding alone.

## III. LINEAR FEEDBACK SHIFT REGISTERS

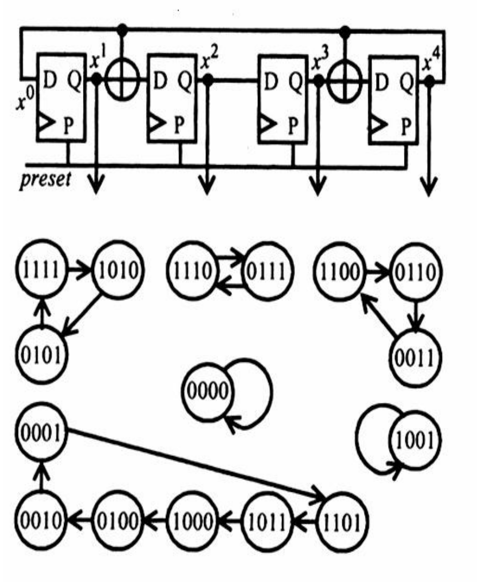
The Linear Feedback Shift Register (LFSR) is one of the most frequently used TPG implementations in BIST applications. This can be attributed to the fact that LFSR designs are more area efficient than counters, requiring comparatively lesser combinational logic per flip-flop. An LFSR can be implemented using internal or external feedback. The former is also referred to as TYPE1 LFSR while the latter is referred to as TYPE2 LFSR. The two implementations are shown in Figure. The external feedback LFSR best illustrates the origin of the circuit name – a shift register with feedback paths that are linearly combined via XOR gates. Both the implementations require the same amount of logic in terms of the number of flip-flops and XOR gates. For high performance designs, the choice would be to go for an internal feedback implementation whereas an external feedback implementation would be the choice where a more symmetric layout.



(a) internal feedback LFSR (b) external feedback LFSR

Fig.1 LFSR Implementations

The value that the LFSR [3] is initialized with, before it begins generating a vector sequence is referred to as the seed. The seed can be any value other than an all zeros vector. The all zeros state is a forbidden state for an LFSR as it causes the LFSR to infinitely loop in that state.



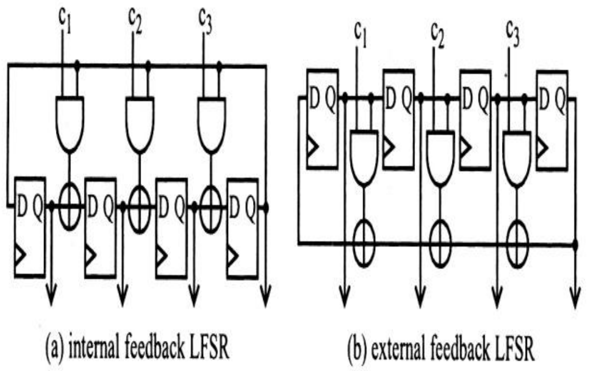
(a) internal feedback $P(x) = x^4+x^3+x+1$

Fig2 Test Vector Sequences.

This can be seen from the state diagram of the example above. If we consider an n-bit LFSR, the maximum number of unique test vectors that it can generate before any repetition occurs is $2^n$ - 1 (since the all 0s state is forbidden). An n-bit LFSR implementation that generates a sequence of $2^n$ – 1 unique patterns is referred to as a maximal length sequence or m-sequence LFSR. The LFSR illustrated in the considered example is not an m-sequence LFSR. It generates a maximum of 6 unique patterns before repetition occurs. The positioning of the XOR gates with respect to the flip-flops in the shift register is defined by what is called the characteristic polynomial of the LFSR. The characteristic polynomial is commonly denoted as P(x). Each non-zero co-efficient in it represents an XOR gate in the feedback network. The $X^n$ and $X^0$ coefficients in the characteristic polynomial are always non-zero but do not represent the inclusion of an XOR gate in the design. Hence, the characteristic polynomial of the example illustrated in Fig.2 is P(x)= $X^4 + X^3 + X + 1$.

***GENERIC LFSR DESIGN :***

Suppose a BIST application required a certain set of test vector sequences but not all the possible $2^n$ – 1 patterns generated using a given primitive polynomial – this is where a generic LFSR design would find application. Making use of such an implementation would make it possible to reconfigure the LFSR to implement a different primitive/non-primitive polynomial on the fly. The control inputs $C_1$, $C_2$ and $C_3$ determine the polynomial implemented by the LFSR. The control input is logic 1 corresponding to each non-zero coefficient of the implemented polynomial [4]



(a) internal feedback LFSR (b) external feedback LFSR

Fig.3 Generic LFSR Implementation.

**LFSRS USED AS OUTPUT RESPONSE ANALYZERS (ORAS):**

LFSRs are used for Response analysis. While the LFSRs used for test pattern generation are closed system (initialized only once), those used for response/signature analysis need input data, specifically the output of the CUT. Fig 2 shows a basic diagram of the implementation of a single input LFSR for response analysis.

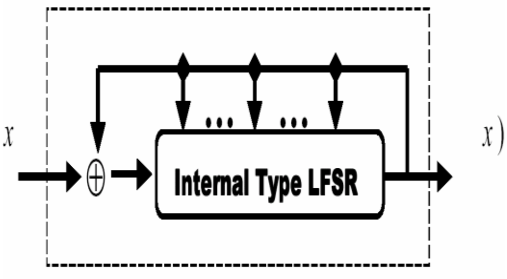


Fig.4 Use of LFSR as a response analyzer

Here the input is the output of the CUT x. The final state of the LFSR is x) which is given by x) = x mod P(x) where P(x) is the characteristic polynomial of the LFSR used. Thus x) is the remainder obtained by the polynomial division of the output response of the CUT and the characteristic polynomial of the LFSR used.

***MULTIPLE INPUT SIGNATURE REGISTERS:***

The example above considered a signature analyzer that had a single input, but the same logic is applicable to a CUT that has more than one output. This is where the MISR is used.

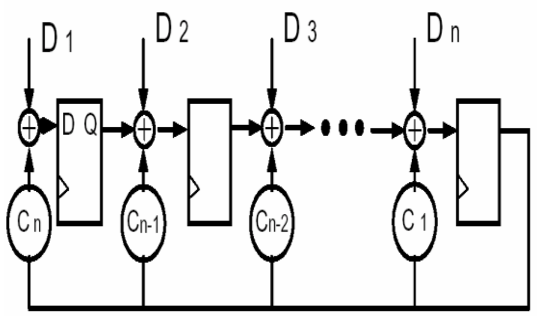


Fig.5 Basic multiple input signature registers

This is obtained by adding XOR gates between the inputs to the flip-flops of the SAR for each output of the CUT. MISRs are also susceptible to signature aliasing and error cancellation. In what follows, masking/aliasing is explained in detail.

***OUTPUT RESPONSE ANALYZERS:***

When test patterns are applied to a CUT, its fault free response(s) should be pre-determined. For a given set of test vectors, applied in a particular order, we can obtain the expected responses and their order by simulating the CUT. These responses may be stored on the chip using ROM, but such a scheme would require a lot of silicon area to be of practical use. Alternatively, the test patterns and their corresponding responses can be compressed and re-generated, but this is of limited value too, for general VLSI circuits due to the inadequate reduction of the huge volume of data. An interesting property of the LFSR with state skipping is that there are no gates modifying the LFSR flip-flop output sequence. From this reason it could be possible that the test pattern decoding LFSR can be shared with the first bits of the parallel scan chains. This arrangement could be used only in cases when the first scan chain bits cannot be overwritten by the functional outputs .Sharing the flip-flops between the de-compressor and scan chains reduces the hardware overhead. Due to complications with the EDA tools [5] adaptation we performed our experiments with separated scan chains and de-compressor only.  The controllability of the LFSR flip-flops can be improved also by using two or more independent input bit sequences (2 or more bit T sin signal). We have verified that for the circuits with approx. one hundred parallel scan chains this solution lead to shortening the test sequence but the amount of stored data in total has grown and lower number of introduced test patterns did not compensate the growing number of tester data and channels. The number of parallel scan chains that are fed from the LFSR is also important from the hardware overhead point of view.

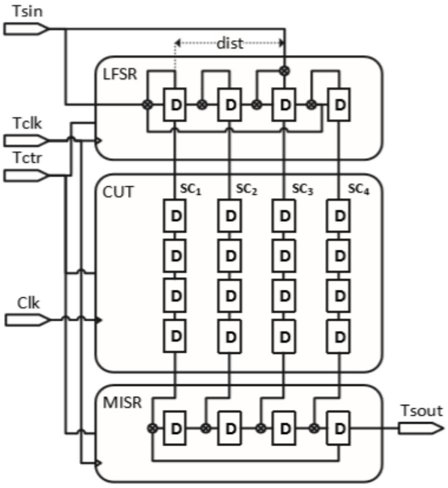
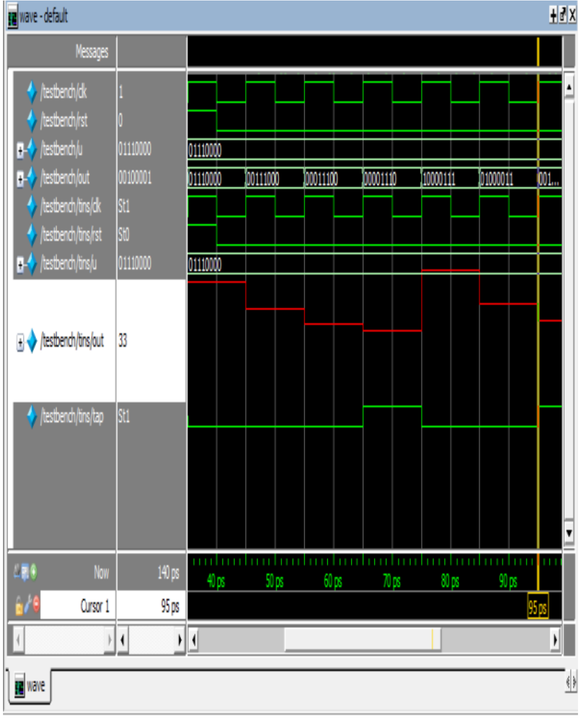


Fig.6 Simplified Scheme Of The Test Equipment

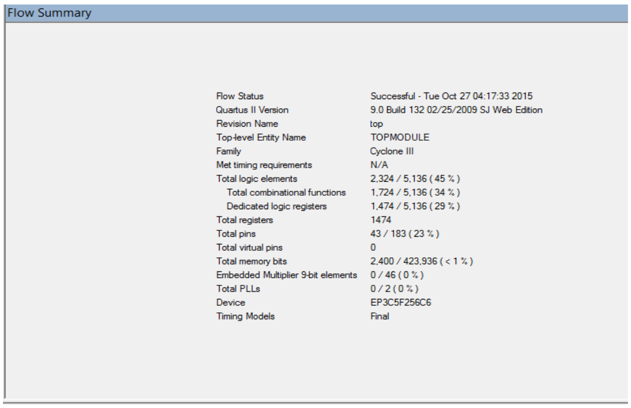
## IV. SOFTWARE IMPLEMENTATION RESULTS

### *a) Functional Verification of Modelsim Output*



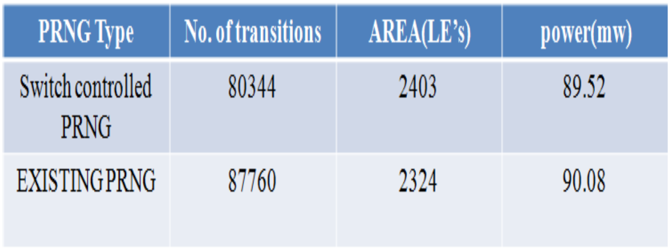
| Messages | |
|---|---|
| /testbench/clk | 1 |
| /testbench/rst | 0 |
| /testbench/u | 01110000 |
| /testbench/out | 00100001 |
| /testbench/tins/clk | St1 |
| /testbench/tins/rst | St0 |
| /testbench/tins/u | 01110000 |
| /testbench/tins/out | 33 |
| /testbench/tins/tap | St1 |
| Now | 140 ps |
| Cursor 1 | 95 ps |

*b) Performance Area*



```
Flow Status                           Successful - Tue Oct 27 04:17:33 2015
Quartus II Version                    9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name                         top
Top-level Entity Name                 TOPMODULE
Family                                Cyclone III
Met timing requirements               N/A
Total logic elements                  2,324 / 5,136 ( 45 % )
   Total combinational functions      1,724 / 5,136 ( 34 % )
   Dedicated logic registers          1,474 / 5,136 ( 29 % )
Total registers                       1474
Total pins                            43 / 183 ( 23 % )
Total virtual pins                    0
Total memory bits                     2,400 / 423,936 ( < 1 % )
Embedded Multiplier 9-bit elements    0 / 46 ( 0 % )
Total PLLs                            0 / 2 ( 0 % )
Device                                EP3C5F256C6
Timing Models                         Final
```

## V. TABLE



| PRNG Type | No. of transitions | AREA(LE's) | power(mw) |
|---|---|---|---|
| Switch controlled PRNG | 80344 | 2403 | 89.52 |
| EXISTING PRNG | 87760 | 2324 | 90.08 |

## VI. CONCULSION

In this thesis work by reducing the number of clock cycles and the number of ATE channels in compression methods with minimal hardware complexity. The efficiency of proposed decompression method proved that it eliminates the LFSR lockout. The proposed skipping LFSR provides similar channel separation as the LFSR with a phase shifter but the hardware overhead is lower than the originally introduced solution of the Smart BIST. The number of LFSR flip-flop XORed in parallel with the test volume and the number of parallel scan chains loaded from the decompressor on the length of test sequence. The efficiency and performance of LFSR is verified using modelsim based functional verification. And decompressor low hardware complexity and non-reduced fault coverage is also proved.

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